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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Timothy N Trop
Trop Pruner & Hu PC
8554 Katy Freeway
Suite 100
Houston, TX 77024

EXAMINER

LEE, CHRISTOPHER E

ART UNIT

PAPER NUMBER

2181

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/541,780

Applicant(s)

NISHIMOTO, STEVE

Examiner

Christopher E. Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: .

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DETAILED ACTION

1. Receipt is acknowledged of the Amendment filed 18th of September, 2002. Claims 16 and 22 have been amended; no claims has been canceled; and no claims has been newly added. Currently, claims 1-23 are pending in this application.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Drawings

3. The drawings are objected to because the timing diagram in Fig. 3 (filed on 18th of September, 2002) is incorrect in light of the specification because the timing T₃ through T₆ is not synchronized with the CLK clock signal (See the details in the Response to Arguments).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. Claims 1-9 and 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter, AAPA] in view of Tjandrasuwita [USPN 6,049,883].

Referring to claim 1, AAPA discloses an apparatus (cell 12 of double pumped bus system in Fig. 1) comprising: a first circuit (latch 16 and latch 18 of Fig. 1 as combined) to receive indications of first data associated with a first data set (i.e., a signal DATA 1 indicating the bits of the first data set; See page 2, line 9) and second data associated with a second data set (i.e., a signal DATA 2 indicating the bits of the second data set; See page 2, line 10); and a second circuit (multiplexer 20 of Fig. 1) coupled to said first circuit to cause said first circuit to (See Fig. 1): in a first mode (i.e., mode of cell 12 embodiment in Fig. 1), communicate indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7) to an output terminal (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a first phase of a clock signal (i.e., negative edge of CLK signal; See page 2, lines 14-15) and communicate

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indications of said second data (i.e., furnishing bits of said second data; See page 2, lines 7-8) to said output terminal (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a second phase of said clock signal (i.e., positive edge of CLK signal; See page 2, lines 17-19). AAPA does not disclose a clock gating apparatus for a mode control, wherein said first circuit to prevent communication of said second data during said second phase of clock signal. Tjandrasuwita discloses a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock gating apparatus, as disclosed by Tjandrasuwita, in said apparatus (i.e., double pumped bus system), as disclosed by AAPA, so that said apparatus could control (i.e., allowing or preventing) said communication of said second data during said second phase. AAPA, as modified by Tjandrasuwita, teaches a second mode, wherein said first circuit (latches in Fig. 1 as combined of AAPA) communicates said indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7 of AAPA) to said output terminal (wire 26 of Fig. 1 of AAPA) in synchronization (See page 2, lines 21-23 of AAPA) with said first phase (i.e., negative edge of CLK signal; See page 2, lines 14-15 of AAPA) and prevents communication (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita) of said second data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) during said second phase (e.g., positive edge of Clock 406 of Fig. 5 from Tjandrasuwita).

Referring to claim 2, AAPA discloses said first circuit comprises: a first latch (bit latch 16 in cell 12 of Fig. 1) to store at least one bit at a time of said first data; and a second latch (bit latch 18 in cell 12 of Fig. 1), at least in said first mode (See the claim 1 rejection in terms of the clock gating), store at least one bit at a time of said second data (See page 2, lines 14-20).

Referring to claim 3, AAPA discloses said first latch (i.e., bit latch 16 in cell 12 of Fig. 1) transfers said at least one bit of said first data in response to a predefined edge (i.e., negative edge) of said clock signal (See page 2, lines 11-20).

Referring to claim 4, AAPA discloses said second latch (i.e., bit latch 18 of cell 12 of Fig. 1) transfers said at least one bit of said second data in response to a predefined edge (i.e., positive edge) of said clock signal (See page 2, lines 11-20) in said first mode (See the claim 1 rejection in terms of the first mode).

Referring to claim 5, AAPA, as modified by Tjandrasuwita, discloses logic (i.e., clock gating in Fig. 5 of Tjandrasuwita) to selectively (i.e., whether EN2 503 is set to enable or disable in Fig. 5; Tjandrasuwita) provide said clock signal to said second latch based on whether said apparatus is in said first (i.e., in case of EN2 is enabled; Tjandrasuwita) or second mode (i.e., in case of EN2 is disabled; Tjandrasuwita).

Referring to claim 6, AAPA, as modified by Tjandrasuwita, discloses said logic does not provide said clock signal (i.e., when EN2 is disabled; Refer to the clock gating logic in Fig. 5, which is consisted of AND gate 503, EN2 input and Clock input 406; Tjandrasuwita) to said second latch in said second mode.

Referring to claim 7, AAPA, as modified by Tjandrasuwita, discloses said logic comprises: an AND gate (gate 503 of Fig 5; Tjandrasuwita) including a first input terminal (EN2 in Fig. 5 of Tjandrasuwita) to receive a mode select signal (i.e., EN2 is enabled when said mode is set to said first mode, and EN2 is disabled when said mode is set to said second mode), a second input terminal (Clock signal 406 of Fig. 5 from Tjandrasuwita) to receive said clock signal and an output terminal (i.e., output of said AND gate 503 of Fig 5. from Tjandrasuwita) coupled to a clock input terminal (CLK of latch 502 of Fig. 5 from Tjandrasuwita) of said second latch.

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Referring to claim 8, AAPA discloses a multiplexer 20 (Fig. 1) including an output terminal (i.e., output of said multiplexer 20 in Fig. 1) that is coupled to said output terminal (wire 26 of Fig. 1) of said apparatus (cell 12 of double pumped bus system in Fig. 1), said multiplexer alternatively selecting said first and second latch in response to said first and second phases of said clock signal (See page 1, lines 24-28 and page 2, lines 21-23).

Referring to claim 9, AAPA discloses said apparatus comprises a double pumped bus circuit (See Fig. 1 and 2).

Referring to claim 15, AAPA discloses a system (double pumped bus system in Fig. 2) comprising: double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data (See page 2, lines 1-3). AAPA does not disclose at least one of said bus circuits being capable of being disabled to prevent bits from at least one of said sets of data from communicated through said at least of said bus circuits. Tjandrasuwita discloses a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said clock gating apparatus, as disclosed by Tjandrasuwita, in said apparatus (i.e., double pumped bus system), as disclosed by AAPA, so that said apparatus could control (i.e., allowing or preventing) said communication of said second data during said second phase. AAPA, as modified by Tjandrasuwita, teaches at least one of said bus circuits being capable of being disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent bits from at least one of said sets of data (i.e., DATA 1 or DATA 2 in Fig. 1 of AAPA) from communicated through said at least of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita).

Referring to claim 17, AAPA discloses each double pumped circuit latches bits (i.e., latches bits using bit latches 16 and 18 in cell 12 of Fig. 1) from one of said sets of data (i.e., DATA 1 or DATA 2 in

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Fig. 1) in response to first edges (i.e., positive or negative edges) of a clock signal (See page 2, lines 11-13) and furnishes indications of said bits in response to second edges (i.e., negative or positive edges) of said clock signal (See page 2, lines 14-20), said first edges being different from said second edges (i.e., a first circuit latches a bit of a first data set at a first edge of a clock signal and a system furnishes a latched bit of a second data set at said first edge of said clock signal, then a second circuit latches a bit of said second data set at a second edge of said clock signal and said system furnishes said latched bit of said first data set at said second edge of said clock signal; See the prior art in the background of AAPA).

Referring to claims 18-19, AAPA teaches said first edges in said system comprises positive edges or negative edges of said clock signal under the condition of mutually exclusive application (See page 2, lines 6-20).

Referring to claim 20, the method steps of claim 20 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 20.

Referring to claim 21, the method steps of claim 21 are inherently performed by the apparatus of claim 2, and therefore the rejection of claim 2 applies to claim 21.

Referring to claim 22, the method steps of claim 22 are inherently performed by the apparatus of claim 2, and therefore the rejection of claim 2 applies to claim 22.

Referring to claim 23, AAPA discloses said method of claim 20, wherein said communicating during said first mode comprise: communicating bits of said first data (i.e., DATA 1 in Fig. 1) in response to first predefined edges (i.e., positive edges) of said clock signal; and communicating a bits of said second data (i.e., DATA 2 in Fig. 1) in response to other predefined edges (i.e., negative edges) being different from said first predefined clock edges (i.e., a first circuit latches a bit of a first data set at a first edge of a clock signal and a system furnishes a latched bit of a second data set at said first edge of said clock signal, then a second circuit latches a bit of said second data set at a second edge of said clock

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signal and said system furnishes said latched bit of said first data set at said second edge of said clock signal; See the prior art in the background of AAPA).

5. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tjandrasuwita [USPN 6,049,883] in view of Applicant Admitted Prior Art [hereinafter, AAPA].

Referring to claim 10, Tjandrasuwita discloses a computer system (computer system 100 of Fig. 3) comprising: a system memory (RAM 304 of Fig. 3); a processor (integrated processor circuit 301 of Fig. 3) coupled to system memory (Fig. 3); and a clock gating apparatus, wherein a circuit (latch circuit 502 of Fig. 5) to prevent communication (i.e., disable EN2 501 of the AND gate input in Fig. 5) of a data (i.e., serial data stream; See col. 6, line 37) during a phase of clock signal (e.g., positive edge of Clock 406 of Fig. 5). Tjandrasuwita does not disclose said processor including: a wire; a first circuit; and a second circuit. AAPA discloses a processor (an apparatus; i.e., cell 12 of double pumped bus system in Fig. 1) including: a wire (wire 26 of Fig. 1); a first circuit (latch 16 and latch 18 of Fig. 1 as combined) to receive indications of first data associated with a first data set (i.e., a signal DATA 1 indicating the bits of the first data set; See page 2, line 9) and second data associated with a second data set (i.e., a signal DATA 2 indicating the bits of the second data set; See page 2, line 10); and a second circuit (multiplexer 20 of Fig. 1) coupled to said first circuit to cause said first circuit to (See Fig. 1): in a first mode (i.e., mode of cell 12 embodiment in Fig. 1), communicate indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7) to said wire (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a first phase of a clock signal (i.e., negative edge of CLK signal; See page 2, lines 14-15) and communicate indications of said second data (i.e., furnishing bits of said second data; See page 2, lines 7-8) to said wire (wire 26 of Fig. 1) in synchronization (See page 2, lines 21-23) with a second phase of said clock signal (i.e., positive edge of CLK signal; See page 2, lines 17-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus, as disclosed by AAPA, in said computer system, as disclosed by Tjandrasuwita, for the

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advantage of reducing the number of wires on said processor of said computer system, which are used to communicate different sets of data (See page 1, lines 9-10). Tjandrasuwita, as modified by AAPA, discloses a second mode, wherein said first circuit (latches in Fig. 1 as combined of AAPA) communicates said indications of said first data (i.e., furnishing bits of said first data; See page 2, lines 6-7 of AAPA) to said output terminal (wire 26 of Fig. 1 of AAPA) in synchronization (See page 2, lines 21-23 of AAPA) with said first phase (i.e., negative edge of CLK signal; See page 2, lines 14-15 of AAPA) and prevents communication (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita) of said second data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) during said second phase (e.g., positive edge of Clock 406 of Fig. 5 from Tjandrasuwita).

Referring to claim 11, Tjandrasuwita, as modified by AAPA, discloses said first circuit comprises: a first latch (bit latch 16 in cell 12 of Fig. 1; AAPA) to store at least one bit at a time of said first data; and a second latch (bit latch 18 in cell 12 of Fig. 1; AAPA), at least in said first mode (See the claim 10 rejection in terms of the clock gating), store at least one bit at a time of said second data (See page 2, lines 14-20; AAPA).

Referring to claim 12, Tjandrasuwita, as modified by AAPA, discloses said first latch (i.e., bit latch 16 in cell 12 of Fig. 1; AAPA) transfers said at least one bit of said first data in response to a predefined edge (i.e., negative edge; AAPA) of said clock signal (See page 2, lines 11-20; AAPA).

Referring to claim 13, Tjandrasuwita, as modified by AAPA, discloses said second latch (i.e., bit latch 18 of cell 12 of Fig. 1; AAPA) transfers said at least one bit of said second data in response to a predefined edge (i.e., positive edge; AAPA) of said clock signal (See page 2, lines 11-20; AAPA) in said first mode (See the claim 10 rejection in terms of the first mode).

Referring to claim 14, Tjandrasuwita discloses logic (i.e., clock gating in Fig. 5) to selectively (i.e., whether EN2 503 is set to enable or disable in Fig. 5) provide said clock signal to said second latch

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based on whether said apparatus is in said first (i.e., in case of EN2 is enabled) or second mode (i.e., in case of EN2 is disabled).

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter, AAPA] in view of Tjandrasuwita [USPN 6,049,883] as applied to claim 15 above, and further in view of Sproch et al. [USPN 6,247,134 B1].

Referring to claim 16, AAPA, as modified by Tjandrasuwita, discloses at least one of said double pumped circuits in said system are disabled (i.e., EN2 501 of Fig. 5 is disabled; Tjandrasuwita) to prevent said bits from at least one of said sets of data (i.e., serial data stream; See col. 6, line 37 of Tjandrasuwita) from being communicated through said at least one of said bus circuits (i.e., disable EN2 501 of the AND gate input in Fig. 5 of Tjandrasuwita). AAPA, as modified by Tjandrasuwita, does not teach alternate double pumped circuits in said system are disabled. Sproch et al. disclose a method and system for pipe stage gating, wherein a stall condition "C" determination circuit 210 (Fig. 8) and a stall signal propagation and clock gating circuit 230 (Fig. 3; i.e., D-latches and AND gates as combined in Fig. 8) alternately disable double pumped circuits (register latches 221,222,223,225 in Fig. 8) when the input operand bit streams are 110011001100... on DATA 1 (bus 242a of Fig. 8) and 001100110011... on DATA 2 (bus 242b of Fig. 8). Refer to col. 12, lines 48-51 for the alternate disabling condition of the clock gates 351,352,353 and 355 in Fig. 8. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said apparatus for alternately disabling said register latches, as disclosed by Sproch et al., in said embodiment of alternately disabling double pumped circuits, as disclosed by AAPA in view of Tjandrasuwita, for the advantage of saving power in said double pumped bus when said bus does not care about said input data, e.g., its results are inconsequential because of equality (See col. 3, line 64 through col. 4, line 3 and col. 12, lines 48-53).

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Response to Arguments

7. Applicant's arguments filed September 18th, 2002 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "The Examiner made an objection to the drawing because reference character '14' has been used to designate both cell and double pumped bus system. However, Applicant does not understand the basis for this rejection." on page 7, the Examiner respectfully disagrees. The Applicant acknowledged the Examiner made an objection to the drawings. (See page 7, lines 17-18 and 21-22.). However, the Applicant states it is a rejection (See page 7, line 19). The Examiner didn't make a drawing rejection, but a drawing objection (See Office Action page 2 composed on 19th of August, 2002; hereinafter First Office Action). And, there are two "reference sign 14's in Fig. 1, on top right hand corner, which was filed on 3rd of April, 2000, because "reference character '14' has been used to designate both cell and double pumped bus system. The Examiner noticed that this had been corrected in Fig. 1, which was filed on 18th of September, 2002.

In response to the Applicant's argument with respect to "The Examiner makes the following objection the timing diagram in Fig. 4 through Fig. 8 is incorrect in light of the specification." on page 7, the Examiner respectfully disagrees. The Applicant discloses the invention is using the CLK clock signal for controlling the inventive double-pumped bus cells. In contrary to the disclosure, the timing T₃ through T₆ is not synchronized with the CLK clock signal (See Fig. 3 on filed 18th of September, 2002).

In response to the Applicant's argument with respect to "The Examiner objects to the specification because it lacks a Summary of the Invention section....thus, Applicant respectfully declines to submit one.", the Examiner agrees. The Examiner stated the guideline for the convenience of the Applicant, which is not an objection, but an illustration of a preferred layout for an utility application (See pages 3-4 of the First Office Action).

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Arguments about “The Examiner fails to establish a prima facie case of obviousness for claims 1, 10, 15 and 20” on pages 9 and 10.

In response to the Applicant’s argument with respect to “The Examiner combines the alleged admitted prior art with Tjandrasuwita in an attempt to establish a case of obviousness with the supply of the missing limitations from the alleged admitted prior art, as disabling a clock signal to a latch circuit”, the Examiner respectfully disagrees. In contrary to the Applicant’s statement, Tjandrasuwita teaches an AND-gate 503 (Fig. 5) in a clock gating circuitry, as disabling a clock signal to a latch circuit 502 (Fig. 5). Disabling the latch 502 (Fig. 5) doesn’t prevent the communication of all data in the Applicant’s invention, but the disabling of a particular phase of a clock signal to disable communication of the second set of data using the combination of the EN2 enabling signal and the CLOCK 406 (Fig. 5), which is similar to the applicant’s invention (See EN 113, AND-gate 112, CLK 131 and Latch 104 in See Fig. 4 on filed 18th of September, 2002).

*In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Applicant states “the Examiner provides no support for a suggestion or motivation for the combination”, the Examiner respectfully disagrees. The Examiner states the proper suggestion/motivation such as,”...so that said apparatus could control (i.e., allowing or preventing) said communication of said second data during said second phase” (See the First Office Action about the rejection of the specific limitations in the claims 1, 10, 15 and 20). Furthermore, the subject matter “AND-gate in a clock gating circuitry” of Tjandrasuwita is well-known to*

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one of ordinary skill in the art of digital circuitry design for the advantage of providing a simple clock gate control (viz., enabling or disabling the clock signal variation).

*In response to the Applicant's argument with respect to "Thus, for at least the reason that a prima facie case of obviousness for claims 1, 10, 15 and 20, withdrawal of the rejections of claims 1-14, 15-19, and 20-23 is requested", the Examiner respectfully disagrees. In contrary to the Applicant's statement, the Examiner successfully establishes a *prima facie* case of obviousness for claims 1, 10, 15 and 20 (See the above claim rejections and the Response to the Arguments), thus withdrawal of the rejections of claims 1-14, 15-19, and 20-23 is not applicable.*

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter S. Wong can be reached on 703-305-3477. The fax phone numbers for the organization where this


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application or proceeding is assigned are 703-305-3718 for regular communications and 703-746-9248 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
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cel/ *CEL*
September 24, 2002


SUMATI LEFKOWITZ
PRIMARY EXAMINER